Preliminary Spec. (Rev.0.6)

16MCDRAM : 16k (1k-WORD X16-BIT) SRAM Cache, TAG, Comparator, built-in Controller 16M(1M-WORD X 16-BIT)DRAM

M5M4V16168ATP

PRELIMINARY
This document is a preliminary specification and some of the contents are subject to change without notice.

DESCRIPTION

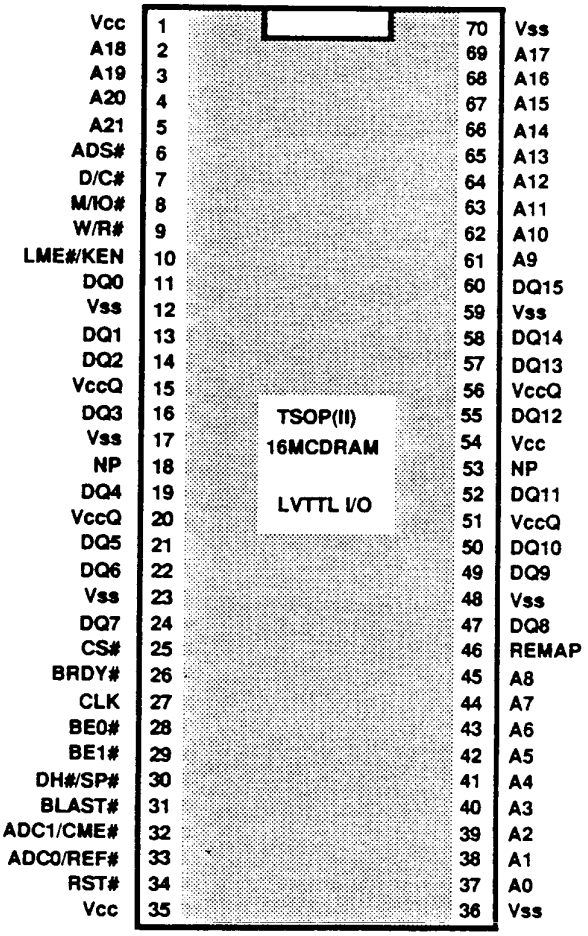
- This 16M-bit Cache DRAM integrates a 1,048576-word by 16-bit dynamic memory array, a 1024-word by 16-bit static RAM as a cache memory (block size 8X16) , TAG memory and cache controller onto a single monolithic circuit. The block data transfer between the array and the data transfer buffer is performed in one clock cycle, a fundamental advantage over a conventional DRAM/SRAM cache system.
- The RAM is fabricated with high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation and low cost are essential. The use of a single-transistor dynamic storage stacked capacitor cell and a six-transistors static storage cell provide high circuit density at reduced cost.

FEATURES

- Direct connection to a microprocessor
- 70 pin, 400mil TSOP (type II) with lead pitch of 0.65mm and package length of 23.49mm.
- Single 3.3V +/- 0.3V Power Supply.
- Internal 4096 refresh cycles every 64ms.
- Synchronous design for precise control with an external clock (CLK).
- Sleep mode is provided for the low power application.
- All inputs/outputs low capacitance and LVTTL compatible.
- Direct connection to a TTL compatible device.

CLK	: Master Clock
CS#	: Chip Select
REMAP	: Remap
DH#/SP#	: Data Hold/Sleep
A0-21	: Address
BE0-1#	: Byte Enable
ADC0/REF#	: Address Control0 / Refresh
ADC1/CME#	: Address Control1 / Command Enable
DQ0-15	: Data Line
ADS#	: Address Status
M/IO#	: Memory or I/O
D/C#	: Data or Code
W/R#	: Write or Read
BLAST#	: Burst Last
RST#	: Reset
BRDY#	: Burst Ready
LME#/KEN	: Local Memory Enable / Cache Enable
Vcc	: Power Supply
Vss	: Ground
VccQ	: Power Supply for output
NP	: No Pin

Pin Out



BLOCK DIAGRAM